



250 MHz Demodulating Log Amp Evaluation Board

DATASHEET

AD641-EB

FEATURES

Single or Dual Device Operation
Transresistance Output Amplifier
Jumper Programmable Input Attenuator
Optional Inverted Output
User Area
Offset Nulling

GENERAL DESCRIPTION

The AD641-EB is an evaluation board for the AD641, Analog Devices' high frequency DC coupled demodulating log amp. The features of the AD641-EB include the following:

- The option of evaluating a single AD641 or cascading two devices to extend the dynamic range
- The option to quickly enable the AD641s' on-board attenuator to evaluate different signal levels
- An additional amplifier to realize a current to voltage converter
- A user area to facilitate the addition of any external components that may be required

These features, combined with the careful layout and decoupling of the board, greatly simplify the evaluation of the AD641.

INTRODUCTION

There are essentially four basic ways to configure the AD641-EB. These include using one AD641 or two, either with or without the input attenuator. Among these four there are several techniques for offset nulling. The AD641-EB comes from the factory configured as shown in fig. 1. This configuration is chosen to give maximum functionality from the onset. The configuration highlights two AD641s cascaded with an inductor at the interstage for offset nulling and no input attenuation used. The following sections outline the details of the remaining possibilities.

CASCADED AD641s

Many of the applications requiring logarithmic compression often demand more than 45 dB of dynamic range. To achieve an extended range two AD641s may be cascaded and their log outputs summed together. The AD641-EB is capable of realizing a circuit similar to that shown in figure 32 of the AD641 data sheet. The first step is to make sure that both Log Out pins of the AD641s (U1 and U2) are connected to the AD846 (U3). This is done by inserting jumpers J6 and J9 in the vertical direction and jumpers J7 and J8 in the horizontal direction (thus grounding

LOG COM). When using cascaded AD641s, significant errors can arise from the input offset voltage and large overall gain. Therefore, use either the feedback or inductor offset nulling techniques as outlined in the AD641 data sheet. The details of implementing these techniques are explained next.

The feedback technique is implemented by including 12.5k resistors in locations R7, R8, R18, and R19. If the input attenuator is used, these resistors should be reduced to 7k each to retain approximately the same level of DC feedback. Also .001µF capacitors should be installed in locations C15 and C16 for AC suppression in the feedback.

Another possible option for offset nulling is the use of an inductor between the two AD641s. This technique eliminates only the offset generated by the first stage. As noted in the AD641 data sheet, this coil will short out the DC component of the output while appearing as a high impedance above 30 MHz. Typically, an inductor of 5µH should be used and may be installed in the two plated through holes provided directly between U1 and U2.

SINGLE STAGE OPERATION

If a specific application requires 45 dB of dynamic range or less, a single stage of compression will be sufficient. Several steps are required to configure the AD641-EB for single device operation. The first step is to remove U2 from the board. Next the output of U1 should be connected to U3 by grounding the LOG COM pin (jumper J7 in horizontal direction) and connecting the LOG OUT pin to the AD846 (jumper J6 in vertical position). When using only one stage, there is usually little need for offset adjustment, but the user still has the option of including such a circuit (see MANUAL OFFSET ADJUST). Operations requiring the input attenuators are described in the following section. This section contains instructions for both single and dual operation modes.

CONFIGURING THE INPUT ATTENUATOR

The AD641 comes equipped with an on board attenuator which may be used to reduce the input signal by a nominal 20 dB thus allowing a full scale input of 2V instead of 200 mV. This section illustrates the steps required to include the input attenuator. These steps have also been summarized in Table 1, JUMPER POSITIONS.

To use the input attenuator take the following steps. First connect the input signal to ATN IN at pin 5 and remove it from +SIG IN at pin 20. Do this by inserting jumper J2 and removing jumper J1. Next, connect the input signal to the first amplifier stage by inserting jumpers J3 and J4 onto the board. Now, because the attenuation resistor provides the required intercept temperature compensation, the on-board compensation circuit should be disabled. This means grounding pin 8 of U1 by including jumper J5 on the board. Note that the intercept temperature compensation circuit of the second device has been permanently disabled since it is never needed.

SIGNAL INPUT

The input to the first AD641 (U1) is accessed via the SMA connector labeled IN and is AC coupled through a 0.1µf capacitor. While this capacitor is not necessary for all applications, it is included to provide convenient DC blocking of any residual offset present in the signal source. Following the input capacitor is a 50 termina-

tion resistor (location R1 or R2) to ground. The combination of these two elements forms a first-order, high-pass network with its half power frequency at 31.8 kHz. When the on board input attenuator is used, the impedance looking into the AD641-EB is much less than 50 (typically 50 ||300). To preserve impedance matching the termination resistor will have to be increased to approximately 60. For this case it is possible to use two 120 resistors in parallel installed in locations R1 and R2. Because it is always good practice to equalize the offset error due to bias currents, as a rule, keep R3 equal to R1 and a resistor in location C3 equal to R2. The exception to this rule is when the attenuator is being used in which case there should be nothing in locations R3 and C3.

Note that for DC or pulse response the input coupling capacitor C1 will have to be removed and replaced with a jumper wire.

MANUAL OFFSET ADJUSTMENT

In certain applications it may be necessary to trim the input offset voltage of a single AD641. If this situation arises, include the following components on the AD641-EB. In the location labeled R4 near the lower left of the board install a 20k potentiometer such as the Bourns 339/844c. In locations R5 and R6 use a 50k, 1/4 watt resistor. For capacitors C2 and C8 use a value of 0.1µf and 100pf respectively. As noted in the AD641 data sheet, the offset may be nulled by applying a zero volt input and adjusting R4 until the logarithmic output reaches a local maximum or minimum. When using the input attenuator R3 and C3 should be omitted and R5 and R6 should be 250k each. The manual offset adjustment is generally not recommended when cascading two AD641s since the high gain (100 dB) and open loop condition will lead to significant output drift. However, the technique may be useful for evaluating performance under controlled conditions. Under any other conditions use either the feedback or inductor offset techniques.

POWER SUPPLIES

The AD641-EB requires two dual power supplies, one of which should be operated at ±5 volts and the other at ±15 volts. The power supply lines may be clipped onto the posts provided on the right side of the board or may be soldered directly onto the printed circuit lands. Each power supply input is diode protected to avoid damage to the active components in case of accidentally reversed wires. Each of the devices on the board is supplied with its own decoupling capacitors and isolation resistors as needed so there is no need for outside decoupling components. The ±15V supply is used to power the AD846 transimpedance amp and should be capable of delivering a minimum of 20 mA. The ±5V supply is used to power both AD641s and should be able to deliver at least 100 mA to the board. Tables 3 and 4 show the recommended and maximum operating conditions for these supplies. An alternative to using two dual supplies is to use one dual supply operated at ±6 volts. In this configuration connect the power supply as shown in figure 4.

OUTPUT SECTION

The output of the AD641-EB is accessed via the SMA connector labeled OUT near the top center of the board. The output is derived by performing a current to voltage conversion using the AD846 transimpedance op-amp (U3) and a single feedback resistor, This resistor (R16=1k) is currently set up to give a slope of 1 volt/decade, but may need to be increased slightly to compensate for slope at higher frequencies (see figure 12 AD641 data

sheet). To calculate the feedback resistance for a given slope and frequency the following expression may be used:

 $R_S = LOGSLOPE/L_V$

where:

Rs is the resistance in k 's LOGSLOPE is the desired system response in volts/decade Ly is the slope current, in mA, from figure 12 of the AD641 data sheet.

Note the values of feedback resistance should not be less than 500 for a transimpedance op-amp such as the AD846 since it may lead to instability. An external capacitor (C9) has been included at the TZ node of U3 to provide high frequency carrier suppression. In effect the capacitor transforms U3 into a first order low pass filter with its break frequency at 1/2 R 16C9. The capacitor may be omitted if averaging at the output is not required. In this case maximum frequency response may be desired and an AD844 should be used in location U3. The AD846 is capable of driving ±10 volts into a 500 load and is current limit protected to 65 mA at 25°C. Note that jumpers J6 through J9 have been provided to allow easy conversion to a complementary output voltage. This output is realized by grounding LOGOUT and taking the output signal from LOGCOM. This means that J6 should be horizontal and J7 should be vertical. When using two stages, the same jumper positions apply for J9 and J8 respectively.

USER AREA

A user area has been provided at the top of the board just to the right of the SMA OUT connector. This area consists of an 8 X 9 matrix of 0.1" on center plated through holes which may be soldered to with external components. Power supply and ground pins are located near the user area for easy access.

		Cascaded Operation			Single Stage Operation		
		Inductor offset adjust		feedback offset adjust		with atten	
		with atten.	without atten.	with atten.	without atten.	with atten.	without atten
	<u>C3</u>		·				
	C15			.001µF	.001µF		
	C16			.001µF	.001µF		
	R3		50Ω		50Ω		50Ω
	RI	120Ω	50Ω	120Ω	50Ω	120Ω	50Ω
	R2	120Ω		120Ω		120Ω	
	R7			5ΚΩ	12.5ΚΩ		
	R8			5ΚΩ	12.5ΚΩ		
	R18			5ΚΩ	12.5ΚΩ		
	R19			5ΚΩ	12.5ΚΩ		
	J1		_				
	J2		-	/		/	
	J3	/		/		/	
- 1	J4					\	
,	J5					/	
	J6	V	V	٧	V	V	ν .
j	J7	H	H	H	Н	Н	Н
	J9	V	V	٧	V		
	J8	Н	Н	Н	Н		
	L1*	✓	/				
COND1	TION	1	2	3	4	5	6

Legend: H = in place horizontally

V = in place vertically = in place

- not in place

Table 1 Jumper and Resistor Settings

^{*} L! may also be replaced by a capacitor for high frequency roll-off but will provide no offset nulling compensation.

^{*} In some instances the dynamic range may be increased by installing a 0.1 µF capacitor In location C3 to decouple the inverting input from stray feedback paths.

Table 2 Functional Description of Jumpers

Jumper Number	Description
J1	connect SMA input to +SIG IN pin (pin 1)
J2	connect SMA input to attenuator input (pin 5)
J3	connect attenuated signal to first amplifier stage
J4	connect inverting input to attenuator
J5	disable intercept temperature compensation
J6	connect Log Out of U1 to output or ground
J7	connect Log Com of U1 to output or ground
J8	connect Log Com of U2 to output or ground
J9	connect Log Out of U2 to output or ground

Table 3 Recommended Operating Conditions

Parameter	min	typ	max	units
Vin with atten. Vin without atten. R C, +15	50 4.5 -4.5	15 -15	±2V ±200mV 	peak peak Ω pF volts volts
+5 -5	4.782 -4.65	5 -5	+7.5 -7.5	volts volts

Table 4 Absolute Maximum Ratings*

Parameter	max	min
+15	+18 V	
-15	-18 V	
+5	7.5 V	
-5	-7.5 V	
Vin.	300mV	-3V
RL	—	0Ω

Absolute maximum ratings are derived from the data sheets of the individual components. For more information consult the respective data sheet.

31	500
92	500
83	500
C2	500
R5	50kO
96	SOKO
A7	12.5kO
98	! 2 5k0
R9	100
RIO	100
RII	4 70
R12	470
R13	4 70
R14	100
RIS	100
R16	1kO
R17	470
RIS	12.5kg
RI9	12.5k0
C9	1000pf
C16	1000pf
C15	1000pf
LI	SuH
All other capacitors	O. Luf

Table 5 Component Values

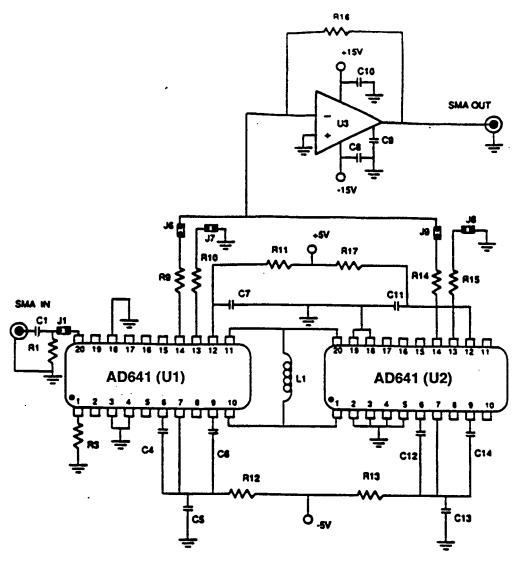


Figure 1 Default Configuration

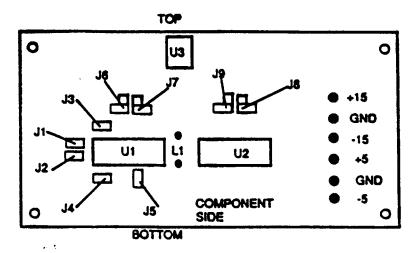


FIGURE 2 Jumper and Power Supply Identification

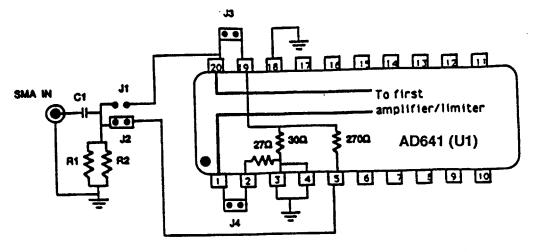


Figure 3 Attenuator Configuration

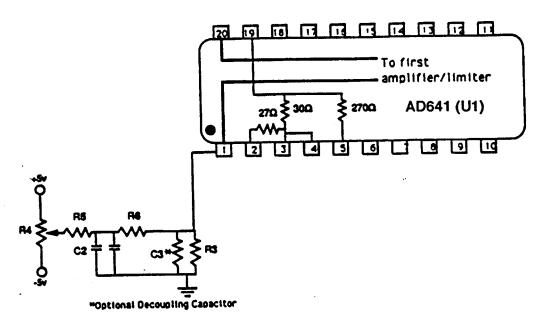


Figure 4 Offset Adjust Circuit

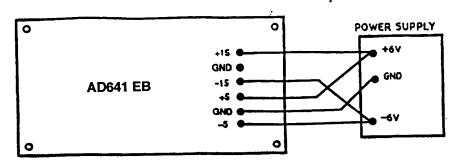


Figure 5 Single Power Supply Connection

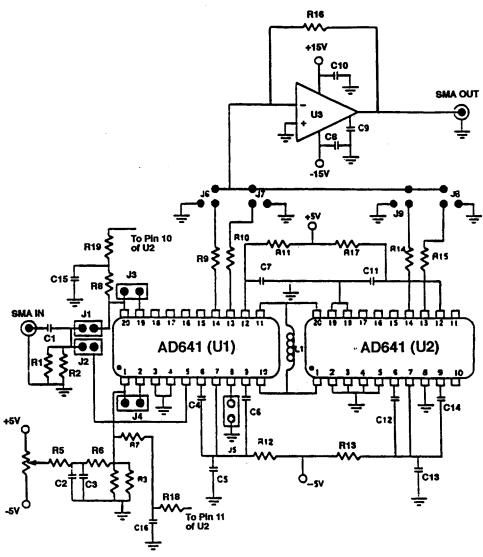


Figure 6 Complete Schematic